High Resolution Coplanar Structures on Multilayer LTCC for Applications up to 40 GHz

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Abstract

The announcement of photoimageable metallisation in conjunction with the conventional screen printing process supports the idea to develop passive components for multichip applications up to an estimated frequency limit of 40 GHz. This technique has been developed by DuPont and is called Fodel^{â}, which has been printed first in a postfired and later in a cofired process on the LTCC Green Tape 951. In the national supported "4M"-project, which is an abbreviation for multifunctional micro- and mm-wave modules, a 4x4-inch LTCC tile with 4 substrate layers and a great number of coplanar, microstrip and stripline test structures and circuits has been designed and fabricated. In the first technology run, the postfired test structures show higher fabrication tolerances, which result in a shift of the Fodel^{â} metal to the inner thickfilm layers and a higher shrinking than expected. In spite of these drawbacks a number of structures and circuits have been evaluated. In a second technology run, the same layout has been fabricated with a cofired Fodel metallisation. The new tiles show an improved alignment between inner and top layer as well as lower shrinking tolerances. Measured and simulated results from both technology runs will be demonstrated and evaluated. Beside the technology aspects, the focus of these investigations lies on the capability of simulation tools for multilayer circuits as well as on applications aspects for RF circuits up to 40 GHz.

1 Introduction

The goal of the LTCC investigations, which is only a small part in the German 4M-project (project number: 16 SV 41 810), is the development of a multichip module for a mm-wave application. The multilayer substrate is used in the transmit, receive and the local oscillator branch to integrate microstrip to rectangular waveguide transitions, MMIC amplifiers, filters as well as frequency multipliers. Before the final multichip module design has been developed by the project partner Daimler-Chrysler Aerospace, a 4x4 inch tile with a big number of test structures and circuits has been designed to investigate this new technology for mm-wave applications. This paper concentrates on those test circuits, which utilise coplanar waveguides on the top layer of the LTCC substrates. The other parts of the whole wafer have been used for microstrip circuitry. The photograph in figure 1 shows the 1x1-inch part of the entire wafer, which carries the coplanar test circuits only. The urgently needed ground to ground connections for the odd mode suppression as well as the transitions in the signal line of a coplanar waveguide on the top to a stripline in a buried layer have been realised with metal filled via holes (see bright dots in the photograph). To achieve experience in the fabrication process, the photoprintable top metal layer has been postfired in a first step with the drawback of misalignment between the outer and inner conductor layer as well as a higher shrinking by firing. These drawbacks could be overcome by cofiring the Fodel conductor. The following chapters will summarise the results of the measurements and simulations of the coplanar test circuits.

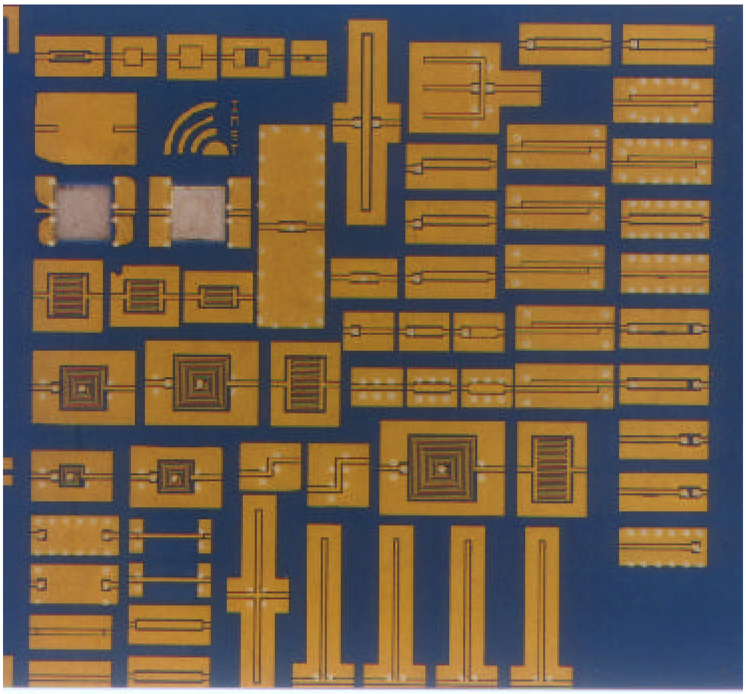

Fig. 1: Photo of LTCC tile with coplanar test structures

2 Transitions

One group of elements deals with the test of transitions from a 50Ω waveguide configuration to another. In the test field for components in coplanar environment, transitions from coplanar to coplanar, from coplanar to microstrip and from coplanar to strip lines have been investigated. In a first step, the geometry of the transition has not been optimised to obtain the frequency limit of a standard transition. Optimised transitions have been published in [1]. Figure 2 and 3 show the return and insertion losses of 4 measured transitions. The first configuration starts at port 1 with a short coplanar 50Ω line, which has a centre line width of 140µm and a spacing to ground of 50µm and is named *CPW1*, while *CPW2* (a 50Ω line, too) has a length of 2400µm, a width of 250µm and a distance to ground of 85µm. Port 2 of the test structure has a small line in the configuration of *CPW1*, so that the effects of the line step appears twice in the measured data. The second transition has a microstrip 50Ω line with a width of 180µm, while the ports are connected to *CPW1*. Both transitions, *CPW1-CPW2-CPW1* and *CPW1-MS1-CPW1* can be used in applications up to 40GHz, because the return losses are close to –20dB or better and the insertion losses are moderate. In contrast, the non-optimised step from the coplanar line *CPW1* to a buried stripline (width = 150µm) is only applicable up to 15GHz. Beyond the matching becomes worse. For the last transition, *CPW1-MS2-CPW1*, a 50Ω microstrip line on a small piece of ceramic substrate has been mounted on the top of the LTCC substrate and has been connected with wire bonds to the coplanar waveguides *CPW1* at the ports, see also figure 8. No compensation for the inductive wire bonds has been used. The measured results show a good matching up to 22GHz and increased losses due to the wire bonds. No accurate models could be found for the simulation of this transitions. That’s why a full wave analysis with the FDTD tool EMPIRE [6] has been performed. The cross view of the test circuit and the simulated and measured return losses are compared in figure 4.

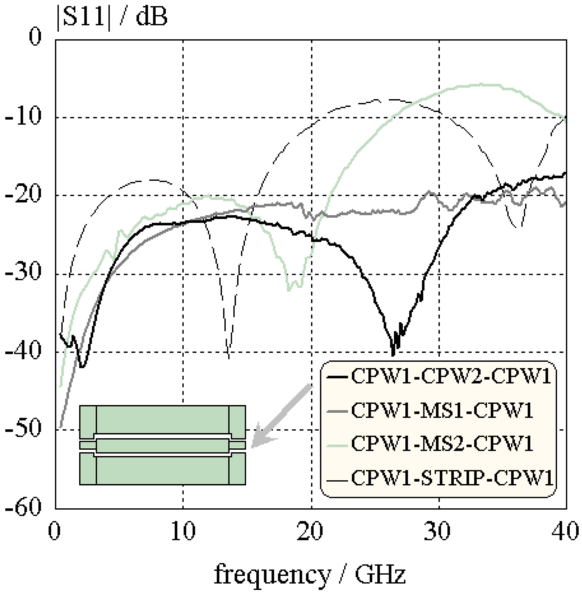

Fig. 2: Return losses of measured waveguide transitions

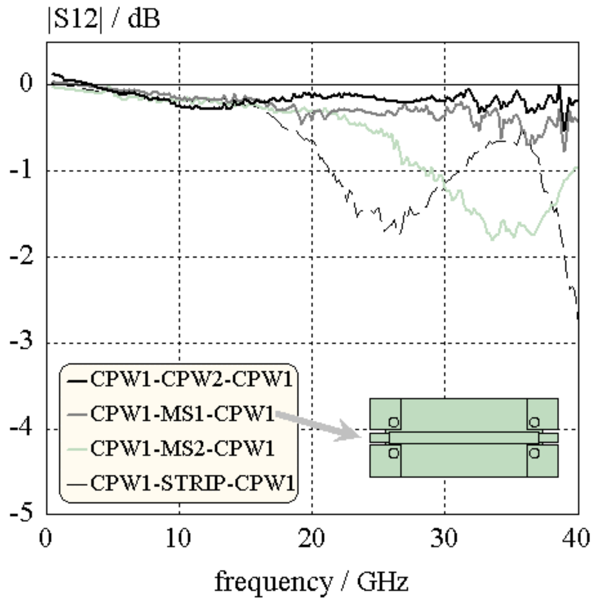

Fig. 3: Insertion losses of measured waveguide transitions

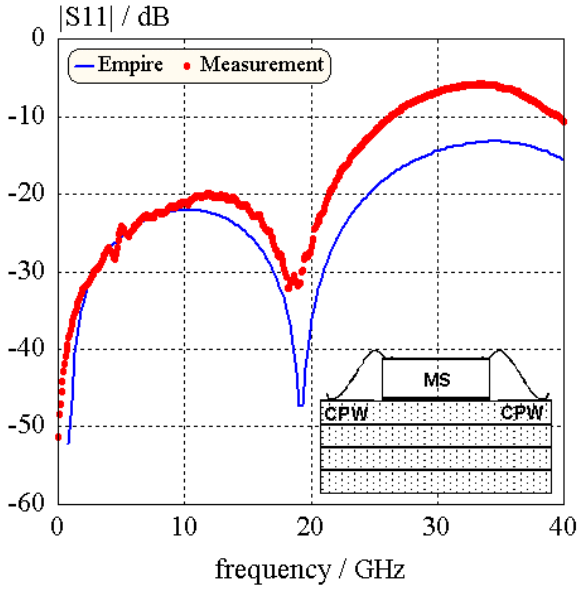

Fig. 4: Measured and simulated (Empire = FDTD method) coplanar to microstrip transition (*CPW1-MS2-CPW1*)

3 Broadside and parallel coupled lines

The next test circuits that will be considered are broadside and parallel coupled lines in a coplanar environment. In both cases the length of the coupling lines is 2400µm. The figures 5 and 6 show the cross and top view of the test circuits as well as the measured S-parameters in comparison with the simulated data up to 40 GHz. In both cases a good agreement could be achieved. The simulations have been performed with a combination of commercial available software (HP-EEsof's SeriesIV, Libra) and in-house software (Coplan for Libra [5] and the FDTD simulation tool "EMPIRE" [6]). The models in Libra („Printed Circuit Board Elements") and Coplan (coplanar lines, discontinuities, lumped elements and coupled lines) use the quasi static Finite Difference method, while EMPIRE utilises a Finite Difference Time Domain formulation. The return and the insertion loss in figure 5 show a resonance peek at about 37 GHz in the simulation only. This deviation from the measured data can be explained by the configuration of the simulated circuit in Libra.

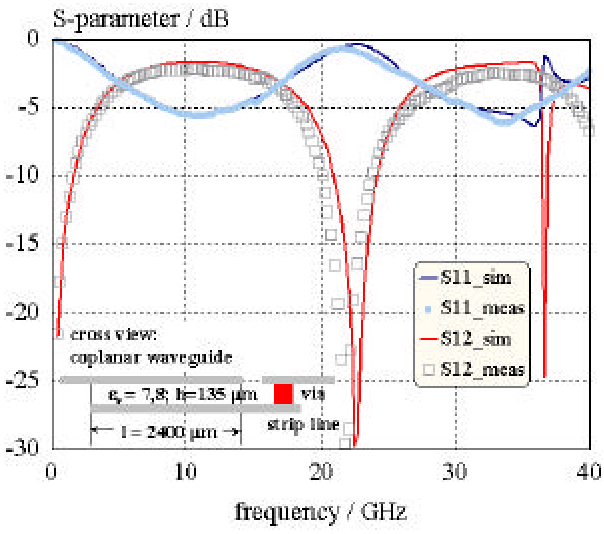

Fig. 5: Measured and simulated S-parameters of broadside coupled lines

The printed circuit board element "PCLIN4" is used for the coplanar waveguide on the top of the substrate (ground – signal –ground) as well as for the buried strip line, which is connected by a metal filled via with to the top conductor. The ports at the ends of the ground strips of the coplanar line have been terminated with ground instead of connecting them with the physical short of the circuit. This results in grounded stubs with resonance’s at 37 GHz.

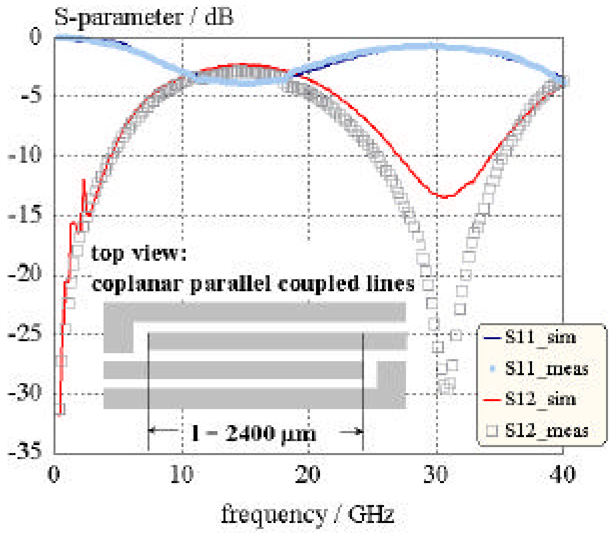

Fig. 6: Measured and simulated S-parameters of parallel coupled lines

4 Resonator stubs

Resonator stubs are excellent for testing a technology, the material parameters as well as the quality of simulation tools. In the photograph of figure 1 a number of test circuits with open stubs can be recognised. Either two stubs in parallel are connected to a cross or one stub is plugged to a t-junction. If coplanar waveguides are used, a ground to ground connection has to be added at each port of any discontinuity. These “bridges” ensure, that the excitation of odd wave modes will be suppressed. This becomes evident, if we consider that odd modes have different signs in the charge on the ground planes on the opposite sides of the signal conductor in coplanar waveguides. This bridge will shorten the opposite grounds and the different charges will be equalised. On multilayer substrates, ground-to-ground connections can easily be fabricated with metal filled via holes and strips in a buried layer. This has been realised in the resonator circuit of figure 7. Four vias around the t-junction and a square conductor plate in a lower layer level are used for the odd mode suppression. In [2] similar resonators had been fabricated on GaAs with and without ground-to-ground connections and in different coplanar line geometry’s. It has been proven, that odd modes excite at higher frequencies and that dispersions effects increase with the frequency and the total cross dimension of the coplanar line. The same effects can be seen at the resonator on LTCC in figure 7. This circuit has been simulated with the same tool: COPLAN for Libra [4,5], which utilises a quasi static finite differences formulation. Dispersion effects can not be determined with this software. Nevertheless, the typical deviation of the resonance frequencies is too high even at lower frequencies (< 15GHz). The reason for this deviation can also result from a tolerance in the dielectric constant of the substrates. Beside this problems the resonance’s have an excellent quality, so that e.g. filters can be designed to 40GHz or even higher.

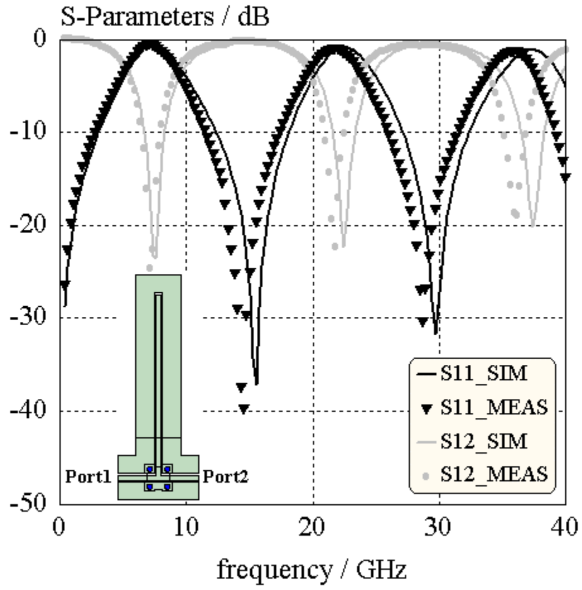

Fig. 7: Measured and simulated Sparameters of a parallel resonator stub

5 Conclusion

The authors have demonstrated with the examples of a number of test circuits, which have been fabricated on a 4 layer LTCC substrate and a photoprintable top conductor, that this technology is capable for the use in multichip modules up to 40GHz or even higher. In total, 100 test circuits for applications in a coplanar waveguide technology have been designed and evaluated. Three fundamental types of structures have been investigated in details in this paper: transitions from coplanar lines to microstrip and striplines, broadside and parallel coupled lines as well as parallel resonator stubs. In all examples, static and full wave simulation tools have been tested to prove the validity of the models for multilayer circuit design.

6 Acknowledgements

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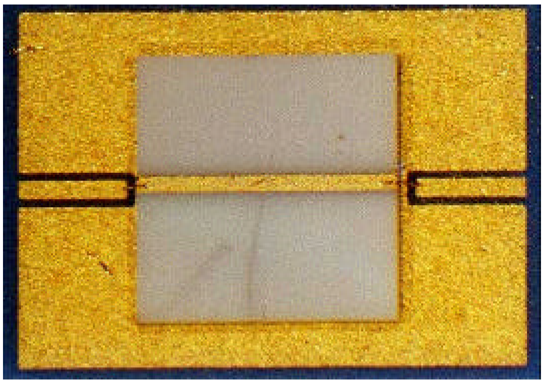

Fig. 8: Photograph of mounted chip connected with wire bonds: microstrip line (w=115µm) on 5 mils Alumina substrate

7 References

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