

# Efficient Band Pass Filter Design for a 25 GHz LTCC Multichip Module using Hybrid Optimization

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**Abstract** — *Multilayer LTCC substrates with screen printed conductors are considered as a key technology for coming RF wireless communication and automotive applications. The direct integration of passive components inside the LTCC environment strongly reduces the costs of a multichip module (MCM). The aim of this paper is to present an efficient way to design a band pass filter for 25GHz with regard to the LTCC design rules.*

**Keywords:** *Filter, RF Design, Optimization, LTCC, Multilayer*

## I. INTRODUCTION

Multilayer LTCC substrates offer the opportunity for low cost, high volume and small size modules for many micro-wave applications since it combines the well established screen printing technique with multilayer ceramic lamination at low firing temperature. Improved materials and fabrication capabilities have been investigated in the Brite-Euram project RAMP<sup>1</sup>. It has been shown that in the manufacturing process a good accuracy could be achieved. This allows the use of LTCC for applications up to a frequency of 30 GHz [1,2]. The integration of band pass filters inside the LTCC also requires high production accuracy. This paper describes how a band pass filter for 25 GHz has been designed with regard to the LTCC design rules. The design has been done by efficiently combining circuit simulation with a fast full wave FDTD analysis. Due to the restricted size available in the multichip module a compact filter layout had to be chosen where couplings between different elements could not be avoided. So the usage of a full wave simulation tool is required for the final design.

<sup>1</sup> RAMP: „Rapid Manufacture of Microwave and Power Modules”, BE-97-4883

## II. FILTER DESIGN

For a point to multipoint Tx-Rx module that is build as a multichip module on LTCC a band pass filter has been designed for a pass band of 24.5 GHz up to 25.5 GHz. The filter has to reduce an unwanted frequency component of a mixer (about 2 GHz below the pass band) with an attenuation of 60 dB. Additionally a 2<sup>nd</sup> product of the mixer at 28 GHz has to be suppressed with an attenuation of 50 dB. To fulfil these high quality specifications a filter has been designed with attenuation poles at  $0.8 \cdot f_0$ ,  $0.9 \cdot f_0$ ,  $1.2 \cdot f_0$ ,  $1.6 \cdot f_0$  and  $1.8 \cdot f_0$ , with  $f_0=25$  GHz. The attenuation poles are obtained by input/output and interstage coupling. Design formulas of [3] have been used to determine the impedances of the tap-, anti-parallel- and parallel coupled structures. Figure 1 shows a top view of the chosen filter structure.

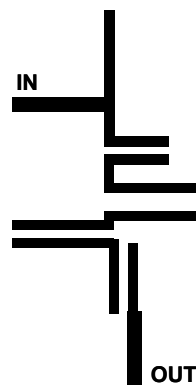


Fig. 1. Top view of the designed filter structure.

In the LTCC environment the filter is realized in stripline technique on a 4 layer substrate with a relative permittivity of 5.9. The layer height is 185 $\mu\text{m}$  and two layers are used as spacing to the ground planes. This results in a 50 Ohm line in a center conductor width of 238  $\mu\text{m}$  and a distance of 370  $\mu\text{m}$  to the ground planes. It was not possible to use only one layer as spacing to the ground because this would result later in to small dimensions for the coupling structures. The LTCC design rules allow a minimal line width and a minimal spacing of 100  $\mu\text{m}$ .

### III. CIRCUIT SIMULATION OF THE FILTER

The circuit simulator ADS<sup>TM</sup> has been used for the simulation of the filter. Ideal elements defined by the characteristic impedances have been used for simulating the open stab, the parallel- and the anti parallel coupled structures. The lengths of the elements have been chosen to obtain a center frequency of 25 GHz. The green curve in Figure 2 shows the simulated insertion loss while the blue curve shows the needed attenuation.

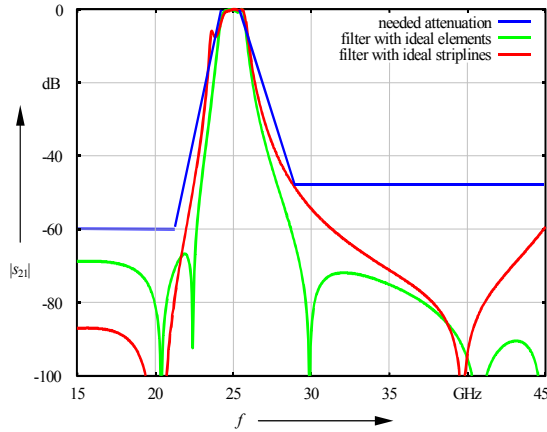


Fig. 2. ADS<sup>TM</sup> simulation results of the filter.

As next step the conductor width ( $w$ ) and the gap width ( $s$ ) of the stripline couplers have been calculated using

$$K(k) = \int_0^{\frac{\pi}{2}} \frac{1}{\sqrt{1 - k^2 \sin^2(x)}} dx, \quad (1)$$

$$k_e(w, s) = \tanh\left(\frac{\pi w}{2h}\right) \tanh\left(\frac{\pi(w+s)}{2h}\right), \quad (2)$$

$$k_o(w, s) = \tanh\left(\frac{\pi w}{2h}\right) \coth\left(\frac{\pi(w+s)}{2h}\right), \quad (3)$$

$$Z_e(w, s) = \frac{K\left(\sqrt{1 - (k_e(w, s))^2}\right)}{4K(k_e(w, s))} \cdot \sqrt{\frac{\mu}{\epsilon}}, \quad (4)$$

$$Z_o(w, s) = \frac{K\left(\sqrt{1 - (k_o(w, s))^2}\right)}{4K(k_o(w, s))} \cdot \sqrt{\frac{\mu}{\epsilon}}, \quad (5)$$

with  $Z_e$  as even mode impedance and  $Z_o$  as odd mode impedance.

The achieved results for the interstage anti parallel coupled lines are,  $w_1=168 \mu\text{m}$ ,  $s_1=187 \mu\text{m}$ ,  $w_2=356 \mu\text{m}$ ,  $s_2=112 \mu\text{m}$ ,  $w_3=148 \mu\text{m}$ ,  $s_3=142 \mu\text{m}$  and for the output parallel coupled lines  $w_4=262 \mu\text{m}$ ,  $s_4=82.7 \mu\text{m}$ . To satisfy the LTCC design rules an optimization was performed in the circuit simulator to increase the slot width of the output coupler to at least 100  $\mu\text{m}$  while fulfilling the specifications. In this step ideal stripline elements have been used to model the filter. The red curve in Figure 2 depicts the achieved results. The required attenuation of 60 dB for the lower frequency and 50 dB for the higher frequency is achieved using a minimal spacing and a minimal line width of 150  $\mu\text{m}$ .

### IV. FULL WAVE OPTIMIZATION OF THE FILTER

The final step in the design was the simulation and optimization of the filter using the 3D full wave FDTD simulator EMPIRE<sup>TM</sup>. The full wave simulator takes the coupling effects between the different couplers into account into account, which are neglected in circuit simulators.

#### A. Efficient Full Wave Simulation Technique

For FDTD Full wave optimization of the band pass filter, more than 250 variants with slightly different geometry had to be simulated. If this is to be done efficiently, the simulation time for one variant has to be less than an quarter of an hour. Very fast FDTD simulations of stripline filters have been achieved by

- 1) Taking into account the field singularities at the edges of the stripline by grid dependent modification of its width [4]. Roughly speaking the line width has to be reduced by 2/3 of the FDTD cell width. Since the transmission line parameters convergence is of second order with regard to the FDTD cell size then, a coarse grid can be used without losing much accuracy.
- 2) Graded Mesh FDTD [5] offers the right amount of geometric flexibility to simulate stripline filter structures with a coarse grid.
- 3) The usage of semi-lumped ports instead of well-known Absorbing Boundary Conditions gives a simulation speedup of approx. 20 percent. A further benefit is, that lumped 50 Ohm ports make S-Parameter results to have a reference impedance of 50 Ohms rather than the frequency dependent characteristic impedance of the transmission line at the port. The ports are realized with a 50 Ohm planar resistor, which has the same width as the stripline. The resistor is in the same plane as the stripline connecting it to a PEC wall. The excitation is done with a current source parallel to the resistor.
- 4) For high quality filters like this, a Resonance Estimation technique [6] allows the simulation time to be reduced by a factor of approx. ten. Here a cybernetic model's parameters are estimated from the voltage and current timeseries FDTD calculates. A much more accurate time-domain to frequency-domain transformation is obtained than with the standard Discrete Fourier Transform (DFT).
- 5) Usage of a well optimized graded mesh FDTD kernel. State of the art FDTD kernels are extended versions of the well-known Yee algorithm [7]. Since this algorithm is simple and short in terms of lines of computer code, heavy optimizations are possible using modern

CPU's floating point extensions (Single Instruction Multiple Data, SIMD). This makes FDTD computation speed only to be restricted by the computer's memory bandwidth on modern CPUs.

### *B. FDTD Simulation of the Filter*

The results achieved by the circuit simulation using stripline elements were used for creating the FDTD model. The simulation results of this initial model show a great difference compared to the circuit simulation. The insertion loss increased from about 1 dB in the circuit simulation to more than 10 dB in the FDTD simulation (see green curve in Figure 5). Responsible for the difference is an unwanted coupling between the different couplers of the filter. Figure 3 shows on the left side the magnitude of the electric field in the region of the stripline at 25 GHz. The color depicts the field strength of the electric field from red (high field values) to blue (low field values). A strong coupling between the first and second interstage coupler can be seen. To reduce the coupling between the second and third interstage coupler, the bottom part of the filter has been mirrored to the other side. The right side of Figure 3 depicts the old layout in gray color and the new layout in black color. The simulation results of the mirrored structure show a great improvement in its electrical behavior. The insertion loss in the pass band decreased from 10 dB to about 3 dB (see black curve in figure 5).

In figure 4, showing the magnitude of the electric field at 25 GHz, it can be seen that the coupling between the first and second interstage coupler has been reduced a lot. Only a slight coupling between the elements is left. This coupling causes the small difference between the circuit simulation and the FDTD analysis of the mirrored structure. Due to this it is necessary to use the full wave simulator for the final optimization.

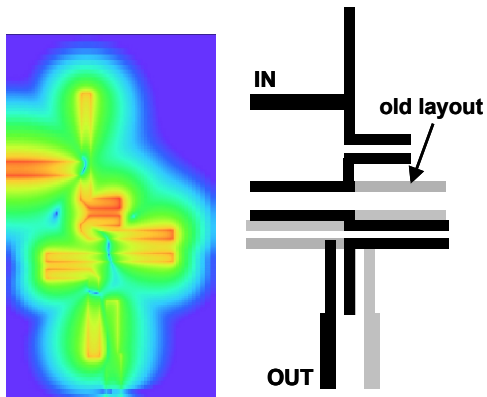


Fig. 3. left: magnitude of the electric field at the filter right: new (black) and old (grey) layout of the filter.

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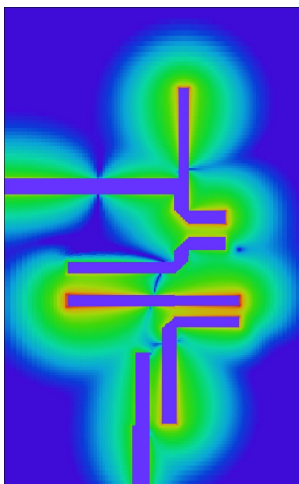


Fig. 4. Magnitude of the electric field in the mirrored filter

In the final optimization the length of the four couplers and the length of the open stub were used as optimization parameters. One simulation needed about 15 minutes and the optimum solution was found within 250 simulations carried out on a PC-

Cluster over night. The simulation results of the optimized structure fulfill the specifications of a pass band with low insertion loss from 24.5 GHz up 25.5 GHz and a high attenuation of the frequencies next to the pass band (see red curve in figure 5). The leakage radiation of the filter into the substrate is below -25 dB and enables the use of this filter in a LTCC multichip module without disturbing other components.

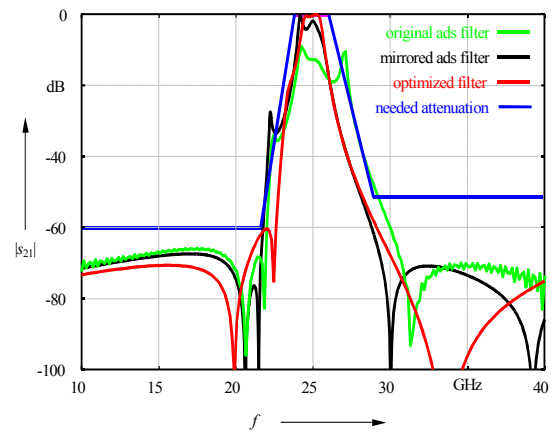


Fig. 5. Full wave simulation results

A rendered view of the optimized simulation model is shown in figure 6.

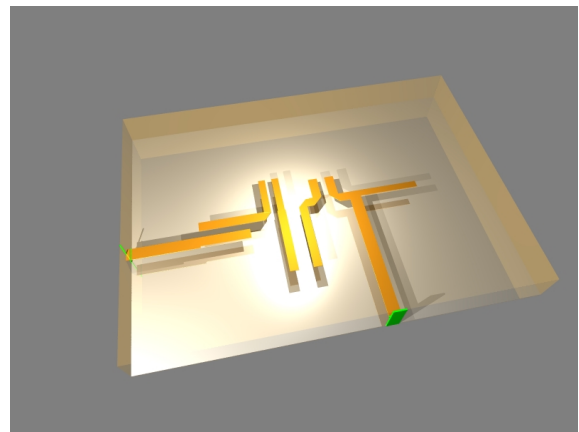


Fig. 6. Rendered 3 D view showing the final filter

## V. REALIZATION

The filter is currently manufactured on a four layer Ferro substrate with gold metallisation on top and silver metallisation inside. The fired height of the four layers is 185  $\mu\text{m}$  for each.

## VI. CONCLUSION

A band pass filter for 25 GHz with high quality specifications regarding attenuation of frequencies next to the pass band (-60 db @ 2GHz offset) has been designed efficiently combining a circuit simulation and a full wave analysis. It has been possible to create a tolerance insensitive layout complied with the LTCC design rules of a minimal spacing and line width of 100  $\mu\text{m}$ . The full wave analysis was necessary to take all couplings into account that the element library of the circuit simulator could not take care off. The couplings between the different couplers could not be prevented due to the high packaging density required in the multichip module.

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