Efficient FDTD parallel processing on modern PC CPUs

Efficient FDTD simulations

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Abstract – In the s first part this paper describes special algorithms for FDTD based field solvers, which increase the simulation speed. Based on a new equivalent circuit for the FDTD calculation scheme a new stability criteria is derived which speeds up the simulations for thin sheets. The new processor generations like Pentium III/Pentium IV and Athlon/Athlon XP have extensions that allow multiple floating point operations within one processor cycle. These extensions can be used to speed up Finite Difference Time Domain simulations. To exploit these extensions efficiently it is necessary to create a processor and structure dependent assembler code for each simulation automatically.

The second part of the paper applies the enhancements invented for the FDTD technique to simulations of a UWB vivaldi antenna. The vivaldi antenna was optimized to achieve a good match and a stable gain over a broadband frequency range. The return loss of this UWB antenna is better than 10 dB for the frequency range from 3 GHz up to 16 GHz. Based on the frequency dependent farfield characteristics the spatio-temporal transfer function of the antenna was calculated. This allows the determination of all relevant quality measures of UWB antennas such as effective gain or ringing.

FDTD, EMPIRE, UWB, timestep, antenna characterization, transfer function

1. Introduction

The FDTD technique is a time domain simulation technique and therefore very good suited for simulations of broadband UWB systems and components. Within one time domain simulation the whole frequency band can be covered. This technique is very memory efficient and allows the calculation of large scale problems. In the standard FDTD technique the timestep gets very small and by this the simulation time very long, if thin elements have to be resolved. The recently developed ADI FDTD technique [1] solves this problem partly, but needs lots of computational overhead. A matrix has to be solved during each timestep, which increases the memory usage and slows down the simulation.

This paper presents a new equivalent circuit for the FDTD, which allows the derivation of a new stability criterion, that allows the usage of a larger timestep in strongly graded meshes without any overhead to the standard FDTD algorithms.

In addition special algorithms are presented additionally, which exploit the SIMD calculation extensions of the new processor generations like Pentium III/Pentium IV and

Athlon/Athlon XP. These extensions can be used to speed up Finite Difference Time Domain simulations, because they allow multiple floating point operations within one processor cycle.

2.   FDTD enhancements

2.1. Improved stability criterion for thin sheets

In the standard FDTD technique the timestep gets very small if very thin sheets have to be resolved within the grid [2]. The new stability criteria for the calculation of the timestep which is presented here allows to choose a larger timestep in strongly graded meshes.
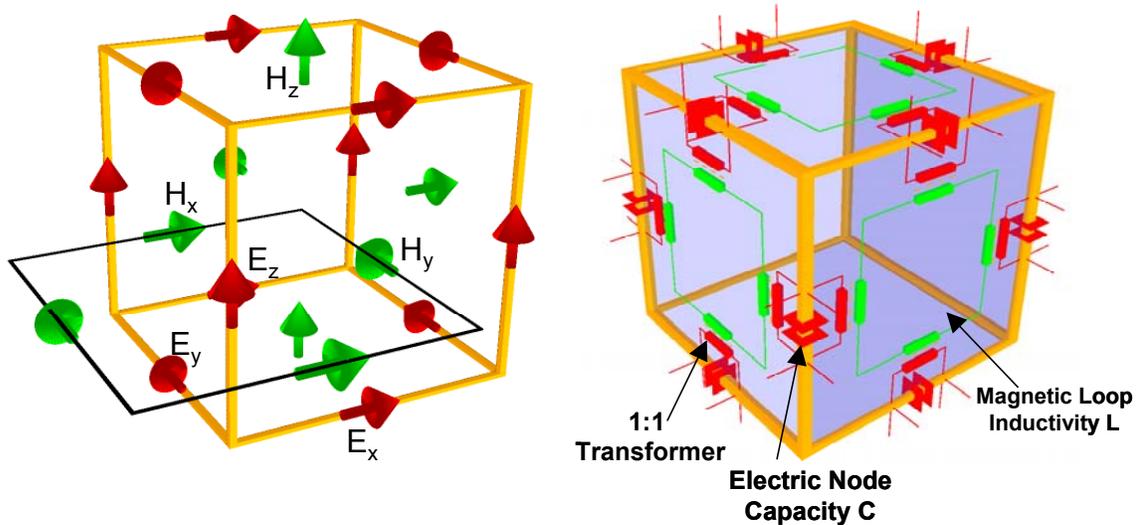

Figure 1: Yee cell (left side) ; FDTD equivalent circuit (right side)

The Yee cell (see left side of figure 1) defines the location of the representative field samples for the electric and magnetic field on the FDTD grid. A new equivalent circuit for the FDTD technique (see right side of figure 1) , which is based on the definitions from the Yee cell, is derived. The electric field nodes are represented by capacities and the magnetic field notes are represented by inductors. The interaction between the electric and magnetic field is realized by transformers. The new criteria for the calculation of the timestep is based on the estimation of the biggest eigen-frequency of the equivalent circuit (1a).

$$\omega_{max} = \max \sqrt{\frac{1}{C} \sum_L \frac{4}{L}} \;\; (1a) \;\; ; \qquad \Delta t \le \frac{2}{\omega_{max}} \qquad (1b)$$

Based on this it is possible to get a new estimation of the upper limit for the timestep (1b). This estimation of the timestep can be in strongly graded mashes up to a factor of 10 larger then the timestep derived from the Courant stability criterion.

2.2. Efficient FDTD simulation by exploitation of modern PC CPUs SIMD extensions

The new processor generations like Pentium III/Pentium IV and Athlon XP/ Athlon 64 have extensions that allow multiple floating point operations within one processor cycle. These Single Instruction Multiple Data (SIMD) extensions can be used efficiently to speed up Finite Difference Time Domain simulations by operating on 4 floating point numbers with one single instruction. To exploit these extensions it is helpful to create a processor and structure dependent assembler code for each simulation automatically. As soon as the structure pre-processing is finished, the CPU is detected and a special CPU dependent assembler code is created for the simulation. Structure dependent code is created which takes into account if e.g. lossy media or non lossy media is considered. That is why in all cases the easiest YEE equations can be solved. Figure 2 shows an example assembler code using Pentium ™ (IV) SIMD commands in the inner FDTD kernel. This part of the assembler code represents one half step in the FDTD time stepping scheme, which updates the electric field components from the already calculated magnetic field components. The upper marked part of the code moves the magnetic field data from the memory to the SIMD registers. Precalculated RAM distances allow a fast memory access and afterwards the sum over 4x4 H-field components is calculated. The next step requires a denormalization of the node capacities to optimize the RAM access. In the last step the 4 E-components are updated and written back to the memory.
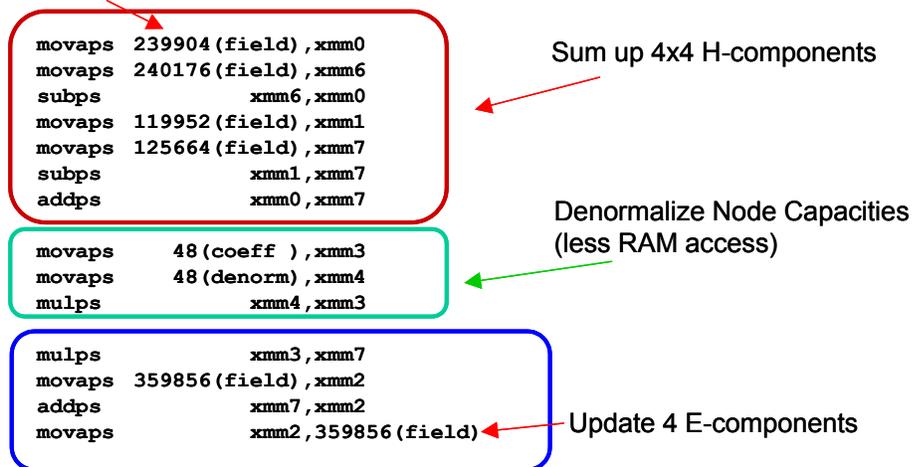
Precalculated RAM distance

```
movaps  239904(field),xmm0
movaps  240176(field),xmm6
subps           xmm6,xmm0
movaps  119952(field),xmm1
movaps  125664(field),xmm7
subps           xmm1,xmm7
addps           xmm0,xmm7
```

Sum up 4x4 H-components

```
movaps      48(coeff ),xmm3
movaps      48(denorm),xmm4
mulps           xmm4,xmm3
```

Denormalize Node Capacities (less RAM access)

```
mulps           xmm3,xmm7
movaps  359856(field),xmm2
addps           xmm7,xmm2
movaps          xmm2,359856(field)
```

Update 4 E-components

Figure 2: Example of an assembler code with Pentium ™ (IV) SIMD commands using 4 Float Numbers/Registers

Due to the high optimization of the assembler code and due to the capability of multiple floating point operations within one processor cycle, the memory interface becomes very important. The L1 and L2 cache can be accessed with a high data rate above 48 Gbytes/s (Figure 3), but their cache size is to small for the FDTD fields. That is way the fields must be fetched from the RAM, which can only be accessed with a data rate of 3.2 Gbytes/s. Due to

this simulation speed is not limited by the clock frequency of the CPU, but by the memory bandwidth. Even in the fastest memory configurations (DDR Ram / Rambus memory) the CPU has to wait for data from the memory.
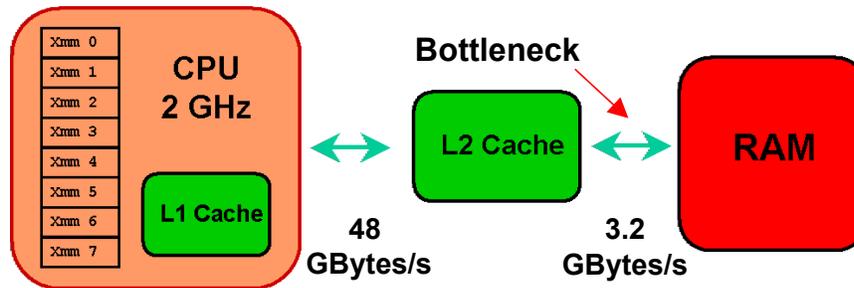
Figure 3: Schematic view of the memory interface from a Pentium 4 CPU

The calculation speed of the optimized FDTD code, implemented in the commercial available Empire^{TM} software [3], for different PC configurations is shown in figure 4. At the moment the fastest PC configuration, which achieves a performance of 60e6 FDTD cells/s, is a 64 bit AMD FX 53 with 2.4 GHz and 400 MHz DDR Ram memory. This in comparison to a PC with an Athlon CPU with 2 GHz and 266 MHz memory quadruples the speed. This speed enhancement within two years time of PC development is a good sign for the future. Additionally is the size of the simulation model, using the new 64 bit PC´s, no longer limited to 4 GB of memory.

Computer	Memory Interface	Performance index
AMD FX53,2.4GHz,64bit, 400MHz DDR	2 x 64 bit on chip	65e6 cells/s
PIV, 3GHz, 400MHZ DDR	2 x 64 bit	45e6 cells/s
AMD Athlon XP 2.6 GHz,nforce2, 400MHz DDR	2 x 64 bit	36e6 cells/s
P4, 2 GHz, Rambus 800MHz	1 x 64 bit	24e6 cells/s
AMD Athlon 2 GHz	1 x 64 bit	15e6 cells/s

Figure 4: FDTD calculation speed for different PC systems

3.   UWB antenna design

The enhancements in the FDTD technique are applied to the design and optimization of a vivaldi antenna. This vivaldi antenna compromises typical UWB behavior like wide bandwidth, low ringing and a stable gain pattern.

3.1. Basic design of the Vivaldi Antenna

The vivaldi antenna [4] is fed by a tapered microstrip line on the bottom side of the substrate which couples the signal by a patch to a slot line that builds the start for the antenna taper.

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The simulation model of the Empire software is shown in the left side Figure 4 and the realized prototype is shown at the right side of figure 5.
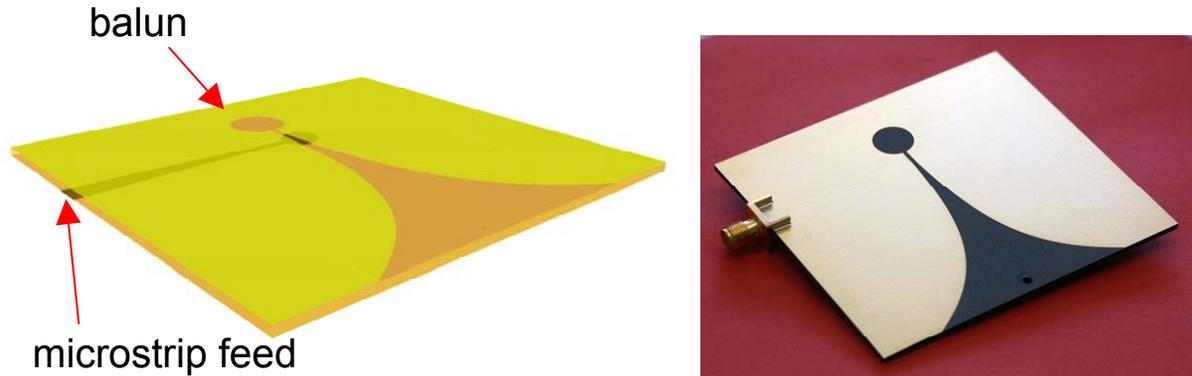

balun

microstrip feed

The excitation is done with a modulated Gaussian pulse of about 500 ps length, which corresponds to a simulation bandwidth from DC up to 15 GHz in the frequency domain. A concentrated current source in parallel to a 50 Ohm resistor is used to excite the pulse at the end of the microstrip line.

The simulation time of the antenna with the optimized FDTD code from the Empire software lies below 3 min and includes the nearfield recording for the nearfield to farfield transformation.

The incident and reflected pulses at the microstrip port one are shown in figure 6. The reflections at about 750 ns are caused by the transition from the microstrip line to the slotline and the reflections at about 1400 ns are caused by the antenna.
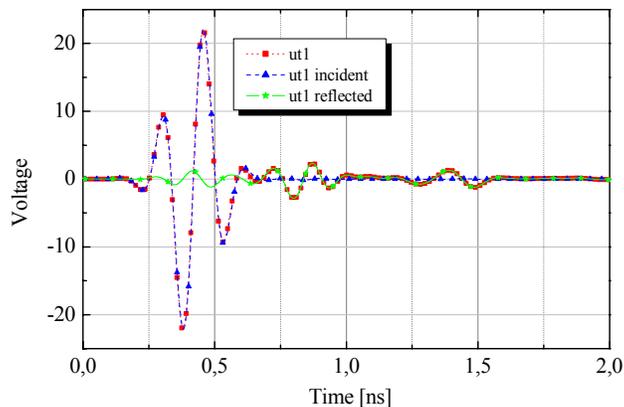

Figure 6: Incident and reflected pulses at the mircrostrip port of the vivaldi antenna

The frequency domain results are created by a discrete fourier transformation (DFT) of the incident and reflected time domain pulses. A comparison between the simulated and measured return loss is shown in the left side of figure 7. A match better than 10 dB is

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achieved for the frequency range from 1.8 GHz up to 10.5 GHz (see left side of figure 7). The agreement between simulation and measurement is very good. The small differences are caused by the coaxial connector which was needed for the measurements.
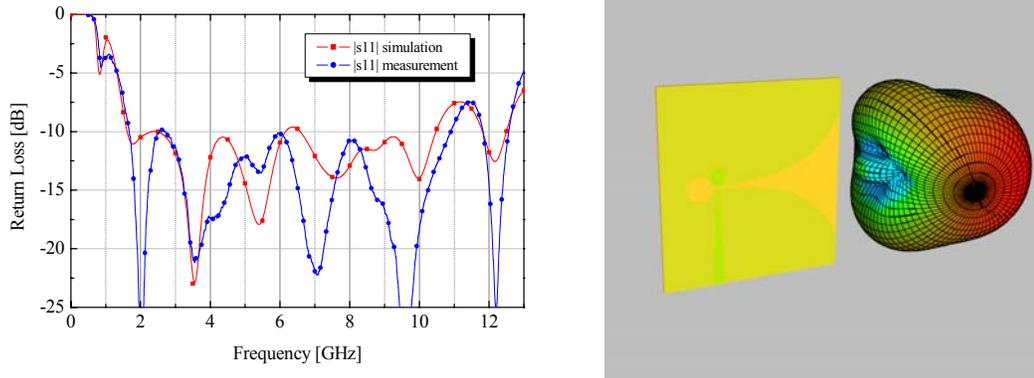

Figure 7: Return loss and 3D farfield pattern at 2.4 GHz of vivaldi antenna

The right side of figure 7 shows a 3D farfield pattern of the antenna. A maximum gain of 5.4 dB is achieved in the direction of the main beam.

3.2. Optimization of the vivaldi antenna

The vivaldi antenna has been optimized to improve its performance. The goal was to achieve a good match and a constant gain over a wide frequency range.
In the first step the taper of the antenna has been optimized. A straight taper was chosen as start value and has been changed to an exponential curve where the radius has been increased step by step. The scattering parameter results from the optimization and the vivaldi antenna with the straight and exponential taper are shown in figure 8.
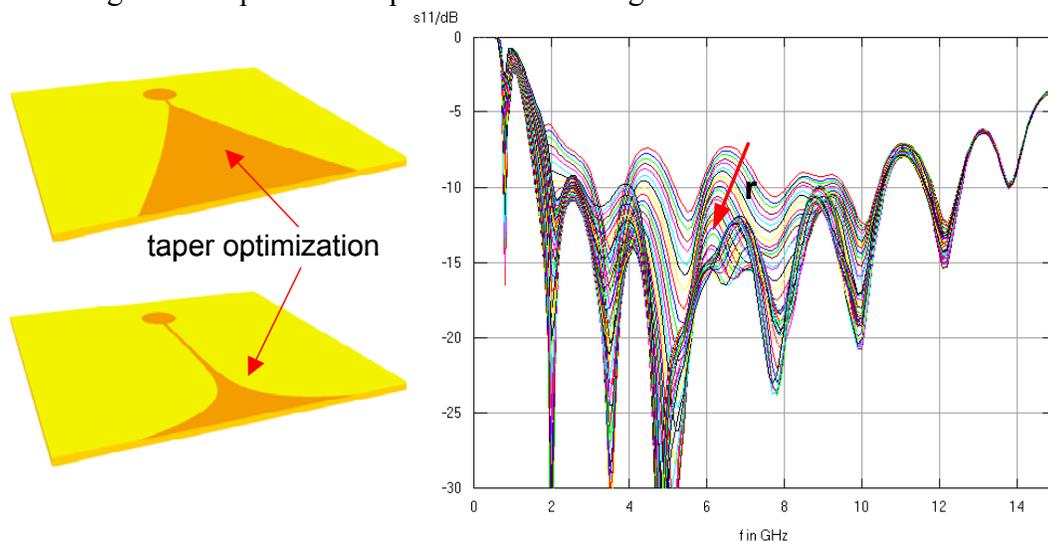

Figure 8: Optimization of the taper from the vivaldi antenna

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It can be seen that the match could be improved between 2 GHz and 10 GHz as the antenna taper is switched to an exponential curve (y=a+b*e^{rx}). A too strong bend in the exponential curve leads to a poor match in the lower frequency range. The match above 10 GHz is not effected by the antenna optimization as the limiting factor for the performance is here the transition from the microstrip feeding line to the slot line.

The transition from the microstrip feeding line to the slot line has been optimized by variation of balun. The diameter d2 from the capacitive patch at the end of the microstrip line and the diameter d1 of the cutout at the beginning of slotline have been optimized. A reduction of the diameters improves the match for higher frequencies while the match becomes a little worse for lower frequencies (see figure 9).
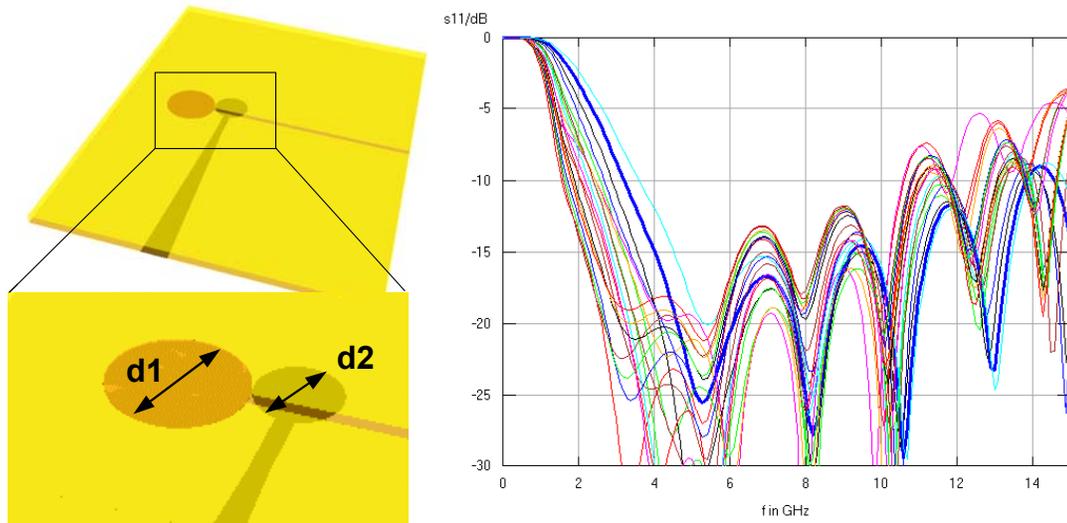

Figure 9: Optimization of the balun from the vivaldi antenna

The automatic optimization needed 60 min for all simulations. A return loss better than 10 dB could be achieved for a frequency range from 3 GHz up to 15 GHz which is a good improvement in bandwidth compared to the not optimized structure (see left side of figure 9). Another benefit of the optimization is a more stable gain curve over the whole frequency range. The gain curve in the main beam direction of the antenna is shown in the right side of figure 10.
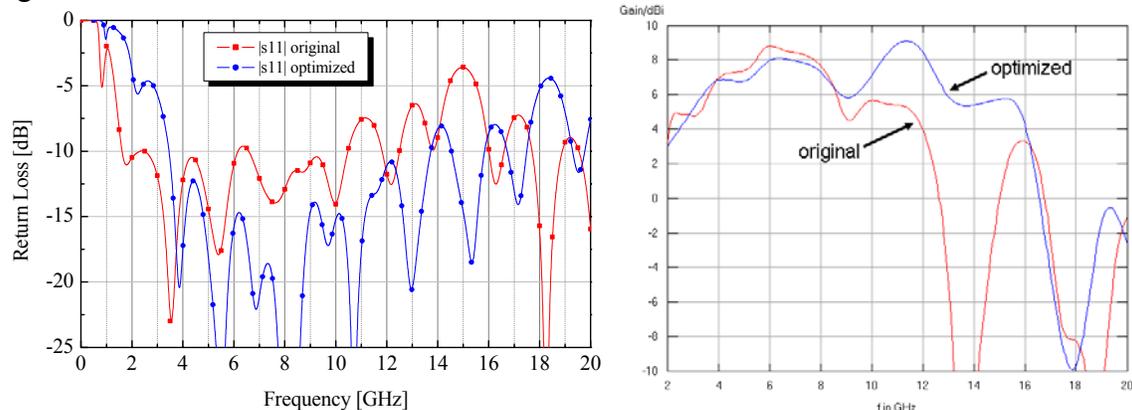

Figure 10: Comparison of return loss and gain between the non optimized and optimized vivaldi antenna

3.3. UWB Antenna characterization using a transfer function

UWB antennas can be characterized very good with their transfer function. This transfer function can be computed easily with the FDTD technique [5]. It is sufficient to do a single numerical simulation of the antenna in transmit mode with recording of the nearfield in a small region around the antenna. Utilizing a nearfield to farfield transformation and the recorded antenna input voltage the transmit transfer function is calculated. The application of the Lorentz reciprocity theorem then yields the receive transfer function from the transmit transfer function. The transfer functions of the antenna allows the calculation of all quality measures of interest either in the frequency domain or the time domain. Figure 11 shows the transmit transfer function of the above described vivaldi antenna in the H-plane. It is visible that antenna has the best performance in the frequency range between 4GHz and 8 GHz
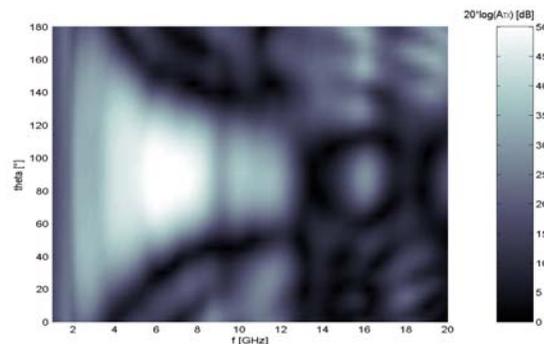
Figure 11: Calculated TX Transfer Function (H-plane)

4.   Conclusion

Several enhancements to the FDTD technique have been proposed. A new stability criteria with strong advantages for FDTD simulations with thin sheets has been derived and new algorithms for parallel processing on modern PC CPUs are presented. These enhancements have been applied to the design and optimization of a UWB vivaldi antenna.

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